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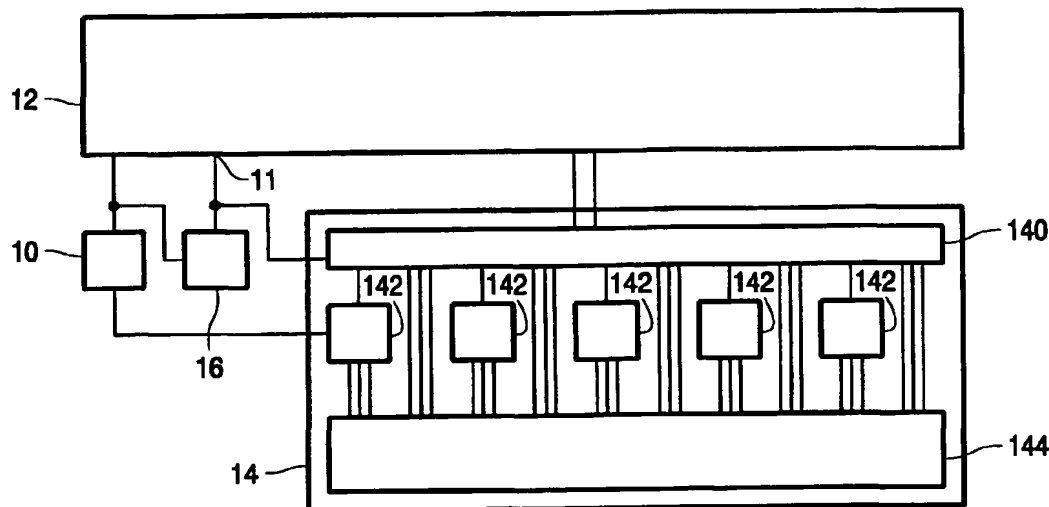
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[Continued on next page]

(54) Title: **VLIW PROCESSOR WITH VARIABLE, ADDRESS RANGE DEPENDENT ISSUE-WIDTH**



(57) Abstract: A data processing apparatus has an instruction memory system arranged to output an instruction word addressed by an instruction address. An instruction execution unit, processes a plurality of instructions from the instruction word in parallel. A detection unit, detects in which of a plurality of ranges the instruction address lies. The detection unit is coupled to the instruction execution unit and/or the instruction memory system, to control a way in which the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range. In an embodiment the instruction execution unit and/or the instruction memory system adjusts a width of the instruction word that determines a number of instructions from the instruction word that is processed in parallel, dependent on the detected range.

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SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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B. FIELDS SEARCHED

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IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, Y	US 2003/065905 A1 (ISHII DAIJI) 3 April 2003 (2003-04-03) paragraph '0011! - paragraph '0012! paragraph '0019! - paragraph '0021!; figures 4,5	1-4, 13-17
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A	EP 0 306 920 A (NIPPON ELECTRIC CO) 15 March 1989 (1989-03-15) abstract	

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☒ Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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